silicon oxynitride (SiON), silicon nitride (SiN), or aluminum oxide.

15. The method according to claim 12, wherein the reaction barrier layer is made of aluminum oxide or titanium oxide.

16. A method of forming a ferroelectric memory device, comprising:

forming a first interlayer insulating layer on a semiconductor substrate;

forming a buried contact structure on the first interlayer insulating layer, the buried contact structure being electrically connected to the substrate via a first contact hole penetrating through a predetermined area of the first interlayer insulating layer;

forming a blocking layer on the buried contact structure and the first interlayer insulating layer to prevent oxygen diffusion of the buried contact structure;

forming a second interlayer insulating layer on the blocking layer; and

forming a ferroelectric capacitor on the second interlayer insulating layer, the ferroelectric capacitor being electrically connected to the buried contact structure through a second contact hole penetrating through a predetermined area of each of the second interlayer insulating layer and the blocking layer.

17. The method according to claim 16, wherein the blocking layer is made of silicon oxynitride (SiON), silicon nitride (SiN), or aluminum oxide.

18. The method according to claim 16, wherein a diameter of the second contact hole is larger than a diameter of the first contact hole.

19. The method according to claim ~~19~~ 16, wherein the buried contact structure is made of tungsten (W).

20. The method according to claim 16, wherein the bit line and buried contact structure are formed concurrently using a conductive material.